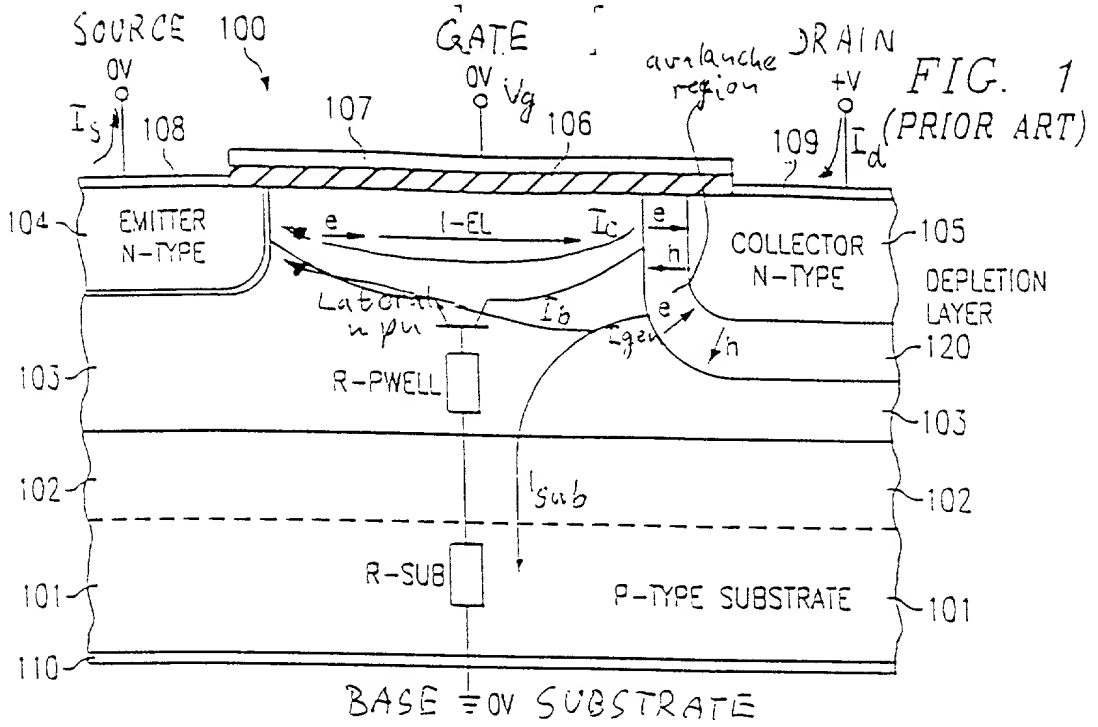

FIG. 1
(PRIOR ART)

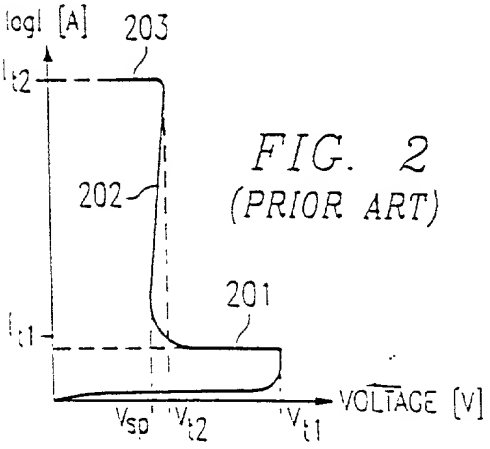

FIG. 2
(PRIOR ART)

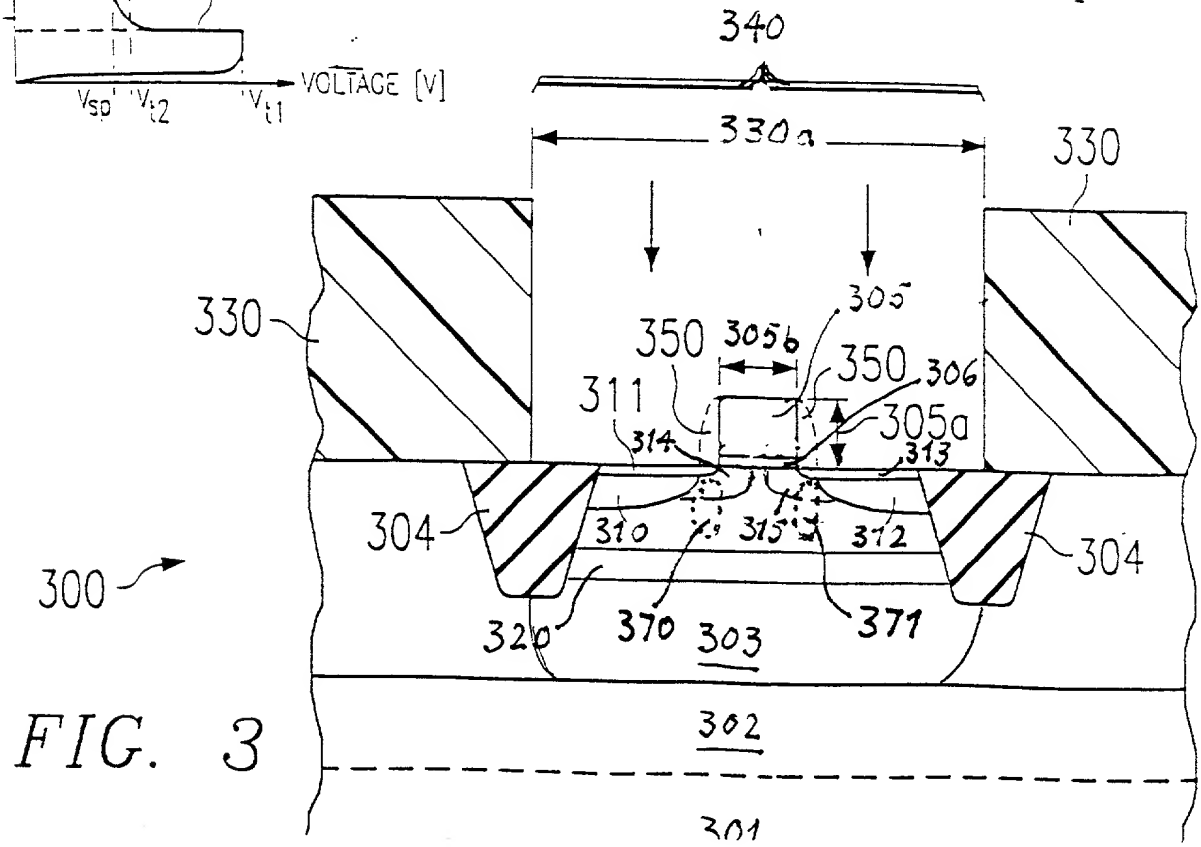

FIG. 3

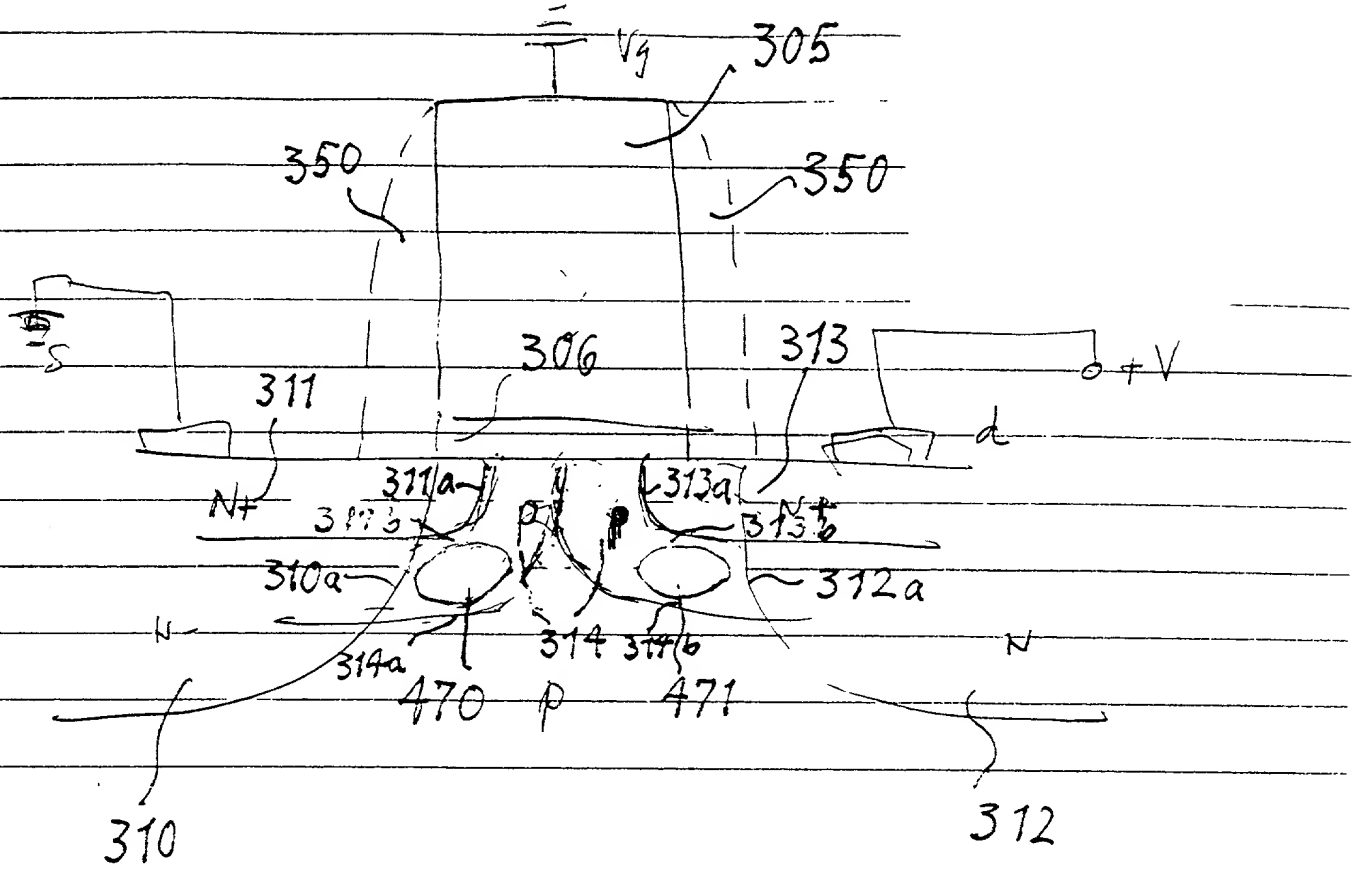
Vg
305
350
350
S
306
313
+V
311
d
311a
313a
N+
N+
310a
312a
N-
N
314a
314
314b
470
P
471
310
312

FIG. 4

Isolation

VT and well implants

Channel stop

Gate definition

NMOS & PMOS LDD & Pocket/Halo implant

Spacer + SD imp

Silicide formation

PMD + Contact formation

Metal deposition pattern

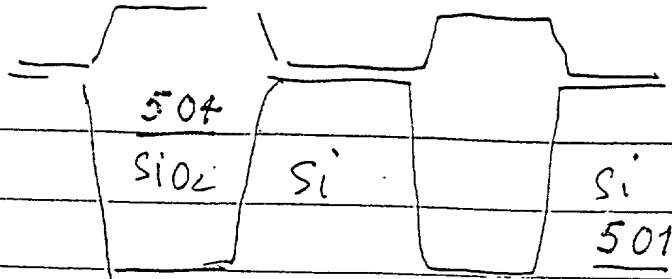

FIG. 5

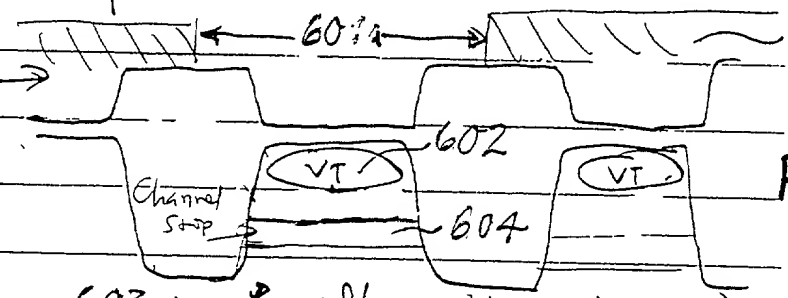

FIG. 6

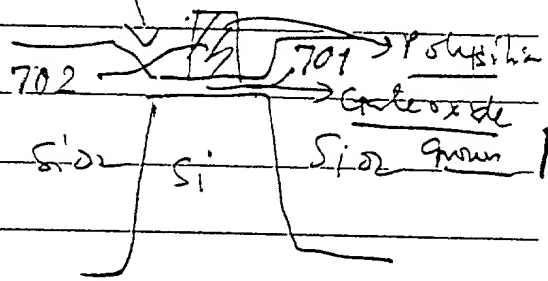

FIG. 7

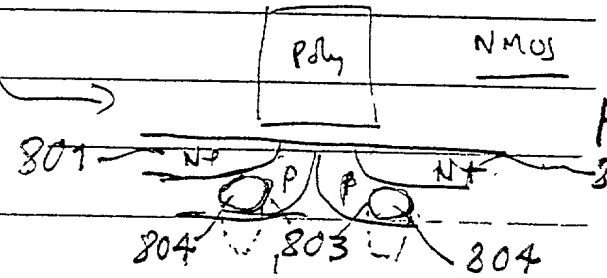

FIG. 8

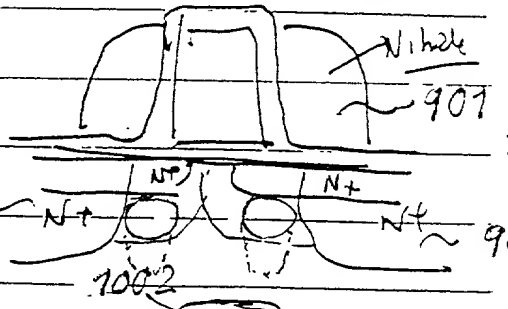

FIG. 9

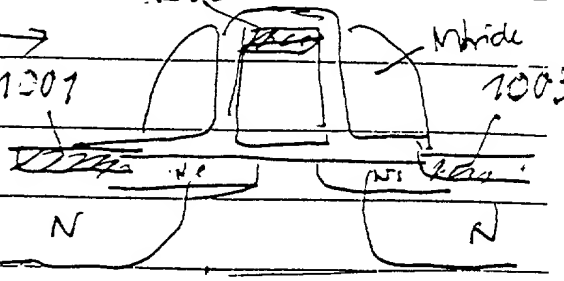

FIG. 10